



PATENT  
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#2

IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicant: Howard H. IRELAND et al. Conf.: 8975  
Appl. No.: 10/366,250 Group: 2133  
Filed: February 13, 2003 Examiner: Unknown  
For: METHOD AND APPARATUS FOR GENERATING BIT  
ERRORS IN A FORWARD ERROR CORRECTION  
(FEC) SYSTEM TO ESTIMATE POWER  
DISSIPATION CHARACTERISTICS OF THE  
SYSTEM

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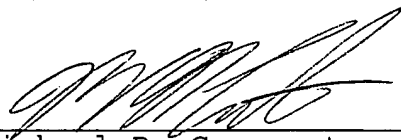
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Respectfully submitted,

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